In the claims

1. (currently amended) A method for fabricating a transistor structure, comprising the steps of:

providing a substrate and forming a lightly doped drain (LDD) region in said substrate;

implanting a first dopant ~~that~~ has a lower dopant concentration than that of the associated LDD region ~~penetrates~~ into said ~~a~~ lightly doped drain (LDD) region to a depth less than a LDD junction depth; and

implanting a second dopant into said substrate beyond the LDD junction depth to form a source/drain region, the implantation of the second dopant overpowering a substantial portion of the first dopant to define a floating region of the first dopant within the LDD region.

2. (previously presented) The method of claim 1, the floating region further comprising a floating ring substantially self-aligned with an edge of a gate of the transistor structure.

3. (currently amended) The method of claim1, further comprising forming the LDD region by implanting a dose of an LDD ~~third~~ dopant that is greater than a dose of the first dopant.

4. (currently amended) The method of claim 1 ~~3,~~ the dose of the first dopant being about twenty-percent or less of the dose of the LDD ~~third~~ dopant.

5. (currently amended) The method of claim 3, at least one of the implantation of the first dopant and the implantation of the LDD ~~third~~ dopant employing tilted angle implants to enhance an amount of overlap between a gate structure of the transistor structure and the LDD region.

6. (currently amended) The method of claim 3, the dose of the second dopant being greater than the dose of the LDD ~~third~~ dopant.

7. (currently amended) The method of claim 3, the implantation of the LDD ~~third~~ dopant further comprising implanting a dose of an n-type dopant in a range from about $1e^{13}$ cm^2 to about $5e^{14}$ cm^2, and the implantation of the first dopant further comprising implanting a dose in a range from about $1e^{12}$ cm^2 to about $5e^{14}$ cm^2 of a p-type dopant.

8. (previously presented) The method of claim 1, the transistor structure is a complimentary metal oxide semiconductor (CMOS) structure that includes a gate having a side edge portion, the floating region being substantially aligned with the side edge portion of the gate.

9. (previously presented) The method of claim 8, the CMOS structure is an n-channel CMOS structure, the first dopant forming a shallow region in the LDD region that comprises a p-type dopant.

10. (previously presented) The method of claim 9, the first dopant comprises boron, and the floating region further comprises a boron floating ring substantially aligned with side edge portion of the gate.

11. (previously presented) The method of claim 8, the CMOS structure is a p-channel CMOS structure, the first dopant defining a shallow region that comprises an n-type dopant.

12. (previously presented) The method of claim 1, further comprising:

forming a gate structure above the substrate, the LDD region and the source/drain region being formed in the substrate generally around the gate structure, the gate structure overlapping at least a substantial portion of the LDD region and the floating ring being substantially aligned with an edge of the gate structure.

13. (currently amended) A method for fabricating a CMOS transistor device, comprising the steps of

forming a gate structure on a substrate, the gate structure having a side edge;

forming a lightly doped drain (LDD) region in the substrate laterally of a channel region and extending beneath said gate structure;

then forming a shallow region in the LDD region having a lower concentration than that of the associated LDD region that extends into the substrate to a depth that is less than an LDD junction depth and spaced from said channel region; and

forming a source/drain region ~~substantially~~, the formation of the source/drain region resulting in forming a floating structure from the shallow region that is located in the LDD region and generally aligned with the side edge of the gate structure.

14. (previously presented) The method of claim 13, the LDD region being formed with a dose of a dopant that is greater than a dose of a dopant utilized to form the shallow region.

15. (previously presented) The method of claim 14, the dose of the dopant that is utilized to form the shallow region is at least approximately twenty-percent less than the dose of the dopant that is utilized to form the LDD region.

16. (previously presented) The method of claim 13, the formation of the LDD region further comprising implanting a dose of an n-type dopant in a range from about $1e^{13}$ cm^2 to about $5e^{15}$ cm^2, and the formation of the shallow region further comprising implanting a dose in a range from about $1e^{12}$ cm^2 to about $1e^{14}$ cm^2 of a p-type dopant.

17. (previously preented) The method of claim 13, at least one of the implantation of the formation of the LDD region and the formation of the shallow region further comprising employing tilted angle implants to increase an amount of overlap beneath the gate structure.

18. (previously presented) The method of claim 13, the formation of the source/drain region being implemented with a dose of a dopant that is greater than a dose of a dopant utilized to form each of the LDD region and the shallow region.

19. (previously presented) The method of claim 13, the CMOS structure is an n-channel CMOS structure, the shallow region comprising a p-type dopant.

20. (previously presented) The method of claim 19, the shallow region comprising boron, the floating structure comprising a boron floating ring substantially aligned with the side edge of the gate structure.

21. (previously presented) The method of claim 13, the CMOS structure is a p-channel CMOS structure, the shallow region comprising an n-type dopant.

22. (previously presented) A transistor structure formed according to the method of claim 13.

23. (withdrawn) A transistor structure, comprising:

a substrate;

a gate structure formed on the substrate, the gate structure having side edges;

a source/drain region having a source/drain extension region, the gate structure overlapping with the source/drain extension region; and

a floating ring within the source/drain extension region substantially aligned with the side edges of the gate structure to mitigate channel hot carrier effects.

24. (withdrawn) The transistor structure of claim 23, the floating ring having a dopant concentration that is less than a dopant concentration of the source/drain extension region.

25. (withdrawn) The transistor structure of claim 23 implemented as an n-channel CMOS transistor, the floating ring comprising a p-type dopant.

26. (withdrawn) The transistor structure of claim 22 implemented as a p-channel CMOS transistor, the floating ring comprising an n-type dopant.

27. (withdrawn) The transistor structure of claim 22, the floating ring extending from a surface of the substrate to a depth that is less than a junction depth of the source/drain extension region.